Semiconductor Memory with Wordline Timing

Abstract of the Disclosure

A semiconductor memory with wordline timing, which links activating a wordline to an isolation signal. The isolation signal is applied to a memory section adjacent the memory section containing the wordline to be activated. Upon such an isolation signal shifting low and isolating the adjacent memory section, a timing circuit triggers a wordline decoder to activate a select wordline. The timing circuit prevents activation of the wordline decoder until the isolation signal is received.